

Nishanth Raghavendra

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EDUCATION

University of Texas at Dallas - Master of Science in Computer Engineering (GPA: 3.7/4)	Aug 2022 – Jun 2024
Visvesvaraya Technological University - Bachelor of Engineering in Electronics and Communication (GPA: 3.6/4)	Aug 2015 – Jun 2019

TECHNICAL SKILLS

Languages: Embedded C, C++, System Verilog, CAPL, Python

Development Software & PLM Tools: Vector DaVinci Configurator and Developer, ETAS Inca, Git, IBM Engineering Requirements Management (RM) DOORS, IBM Engineering PLC Management, Aspic, IBM Clearcase, AWS IoT Hub, JIRA Confluence, Xilinx Vivado, Cadence, Keil Microvision

Simulation, Analysis & Testing Tools: CANalyzer, CANoe, ATI Vision, MATLAB, Simulink, CANdb++ , DET, dSpace, Winldea – iSystem, Lauterbach Trace32, Vector Cast, LDRA, Gem5, JTAG, vFlash

OS: Windows, Linux, Unix, AUTOSAR OS (Vector MICROSAR, ETAS RTA-OS, EB tresos AutoCore)

CORPORATE EXPERIENCE

Platform Software Engineer <i>Ford Motor Company (C2C Cognizant Technology Solutions, USA)</i>	Aug 2024 - Present Dearborn, MI
<ul style="list-style-type: none">Developed and configured the Basic Software (BSW) Communication Stack using Vector DaVinci Configurator tool for over 50 Classic AUTOSAR-based Powertrain Control Module (PCM) applications in a Linux environment using IBM Clearcase tool.Integrated low-level drivers (MCAL) for CAN, SPI, and Watchdog peripherals in C source files to interface with the Firmware – various Powertrain ECUs, facilitating testing and debugging of CAN signals using Vector CANoe and DET tools.Implemented about 30 new signals for Subnet and CAN FD, designed over 25 conformance test suites (CMA) for PCM Control program releases, and validated DBC files with detailed test reports against signal requirements, enhancing subsystem release efficiency.Utilized Agile Scrum methodologies to enhance team collaboration and efficiency through daily stand-up meetings. Managed version control using GitHub.	

Automation and Active Safety (ADAS) Intern <i>Daimler Truck North America</i>	Jun 2023 - Aug 2023 Portland, OR
<ul style="list-style-type: none">Conducted calibration and HIL testing using dSpace Control and Automation Desk for radar ECUs, developing detailed deliverables documentation. Performed systematic false positive analysis for front radar's brake assistance feature by applying clustering techniques on Telematics Unit data, with results visualized in Power BI to ensure DFMEA - ISO 26262 FuSa compliance.Streamlined optical test bench assembly, optimizing setup efficiency and enhancing key image processing attributes to calibrate camera sensor performance.Optimized STOP sign recognition and blind spot detection by refining real-time data from in-vehicle testing and implementing C-based CAPL script, improving detection accuracy and system reliability.	

Software Engineer <i>Veoneer (now Magna Electronics Inc.)</i>	Aug 2019 - Jun 2022 Bengaluru, India
<ul style="list-style-type: none">Designed and implemented over 250 Embedded C unit tests within Software-in-the-Loop (SIL) testing processes for GM Monovision and Night Vision Camera ECUs (Tc27x and Tc23x ARM microcontrollers), ensuring compliance with MISRA and AUTOSAR guidelines to significantly enhancing system robustness.Developed Diagnostic Communication Stack (DCM) in the BSWCM Layer using Vector DaVinci for Stereo Multipurpose Vision Camera ECU, ensuring acknowledged CAN communication between the RTE Layer (diagnostic APIs) and the physical layer (testing tools), including OS (RTOS) and runnable mapping for each task.Debugged and optimized Diagnostic Event Management (DEM), handling DTCs applying ISO 14229 using tools such as Lauterbach and CANalyzer to enhance error-free data transfer and improve ADAS features like Lane Keep Assistance and Blind Spot Detection.Implemented CI/CD pipelines using Jenkins and developed python automation to optimize Bazel builds and payload updates, significantly reducing production build time and RAM usage after each build.Collaborated with a cross-functional team on requirement analysis using IBM DOORS, and functional safety ASIL mapping for various platform features, following the V-cycle development approach.Attended a Model-in-the-Loop (MIL) workshop using MATLAB/Simulink, gaining hands-on experience in model-based testing, control logic validation, and early-stage debugging before SIL testing.	

ACADEMIC PROJECTS

Real-Time Implementation and Evaluation of Adaptive Dynamic Range Optimization (ADRO) for Hearing Enhancement
<ul style="list-style-type: none">Engineered a C code in an ADRO framework using an Android Shell, leveraging signal processing across 32 frequency bands for real-time gain adaptation. Optimized gain mapping with MATLAB-based spectral analysis, adaptive filtering, and dynamic range compression, achieving -30dB to -40dB attenuation in low frequencies and stable -5dB to +5dB gain in mid-to-high ranges for enhanced speech intelligibility.
IoT Temperature Monitoring with Enhanced Facial Recognition
<ul style="list-style-type: none">Developed a Raspberry Pi-based IoT system integrating facial recognition and temperature monitoring with optical machine learning, achieving 100ms response time, 90% accuracy, and real-time AWS data storage via MQTT.

CERTIFICATIONS & AWARDS

Artificial Intelligence and Machine Learning Fundamentals (Cadence), Basic Static Timing Analysis V3.0 (Cadence)
Best Teamplayer of the Quarter (March 2021 - Veoneer)